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Technical Report

HPM7177 EVALUATION (PRELIMINARY)

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Distribution List:

- **TE-EPC**

Reference(s) :

- HPM7177 Design Proposal – EDMS 2169202 V1
- HL-LHC Power Converter Requirements - EDMS 2048827 V3
- Commercial ADC testing for HL LHC - EDMS 2022261 V1

History of Changes

Rev. No.	*Date*	*Pages*	*Description of Changes*
1.0	2019-12-17	12	Document creation

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1. Overview

4 prototype units of HPM7177 were received on 15.10.2019. All units passed the initial functional tests. One mainboard was returned to the workshop for replacement of IC3 (-2.5 V negative voltage regulator). Minor changes were made on the mezzanine boards (see Section 8 for details).

Minimum-functionality firmware was developed for the two Microblaze cores running in the FPGA. Temperature regulation was implemented as a simple PI algorithm. Data readout was done using the NI PXIe chassis and the 8-channel optical interface board. 10 kHz synchronization pulses were provided by the PXIe system.

The power consumption was measured to be approximately 3.3 W per unit, excluding the power needed for the Peltier module (see Section 4.3.) Out of that total figure, about 1 W is consumed by the ADC mezzanine, and ≈0.9 W by the FPGA and digital circuits. The rest is mostly lost on linear voltage regulators.

2. Noise

2.1 Broadband noise

Broadband noise was measured with shorted inputs (on-board MUX short to GND). The ADC contribution was measured with internal ADC short (internal ADC MUX short). The attenuator contribution was calculated as the geometric difference of the two. Results are given in Fig. 1 and Table 1.

The white noise level is higher than in the previously measured prototypes. The reason is the mode of operation of the ADC. In order to guarantee synchronization to external 10 kHz pulses with sufficient time margin, the internal filter of the ADC must be set to a higher cut-off frequency. It leads to aliasing of broadband noise and increase in the noise floor. Despite this effect, the noise floor is still low and well within HL-LHC requirements.

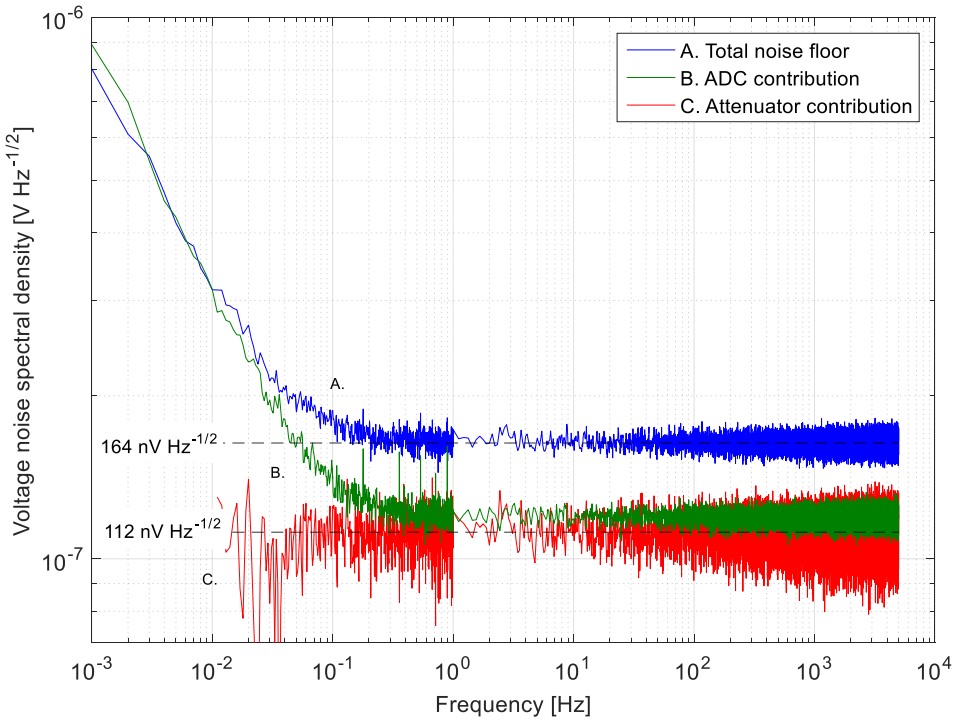

Fig. 1. Noise spectra from 1 mHz to 5 kHz, with separate contributions of the ADC and the input attenuator

Table 1. White noise estimates up to 5 kHz

Measurement	White noise density [nV $Hz^{-1/2}$]	RMS noise from 0.1 to 500 Hz [ppm_{RMS}]
Digitizer total	163.4 ± 4.4	0.36
ADC only	119 ± 3.1	0.27
Attenuator only (calculated)	112 ± 7.3	0.25

2.2 LF noise down to 1 mHz

Low-frequency noise was measured with shorted inputs and with +10 V from a PBC. Results are fully consistent with those from earlier prototype versions. The integrated noise from 1 to 100 mHz is safely within the HL-LHC requiremenets.

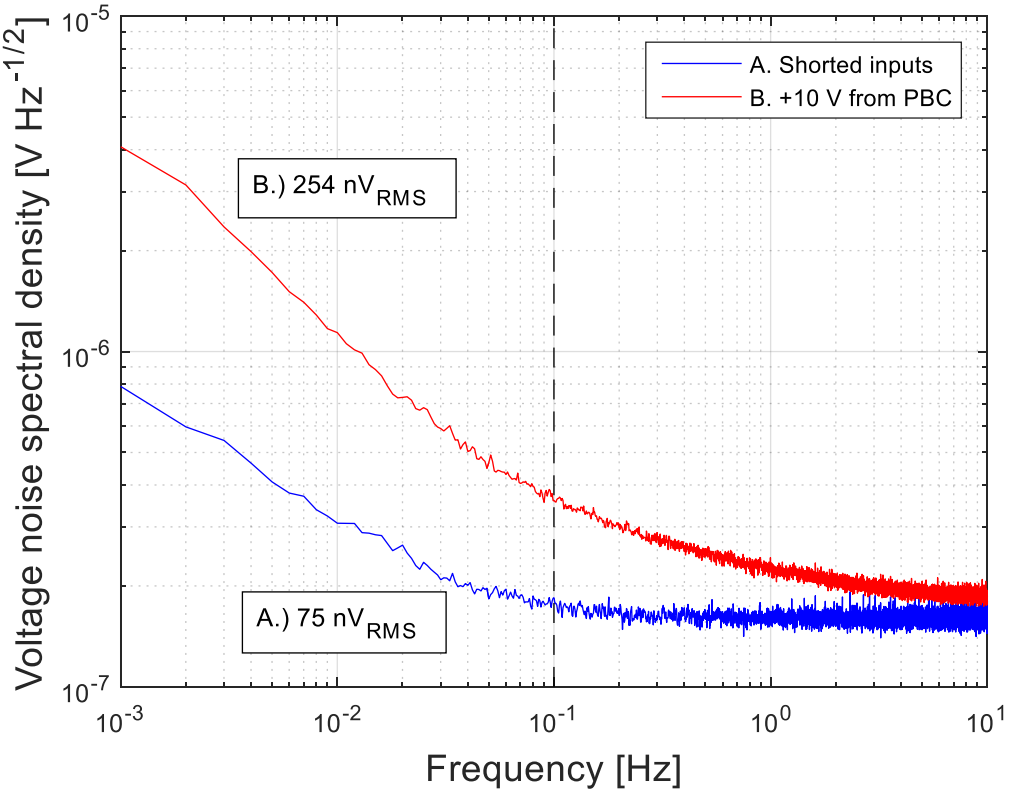

Fig. 2. Low-frequency noise spectra. Integrated RMS noise is given for the frequency band of (1-100) mHz

2.3 Noise below 1 mHz and 12-hour stability

12-hour stability was measured in the oven against a single PBC over 5 days. Results are given in Fig. 3 and Table 2. The measurements were downsampled to 1 Sa/s in the PXIe FPGA and then recorded. They were further downsampled by a factor of 100 in MATLAB, yielding effective upper bandwidth cut-off of about 10 mHz. The spread of Vref voltages is evident in Fig. 3, as the gains were not individually calibrated.

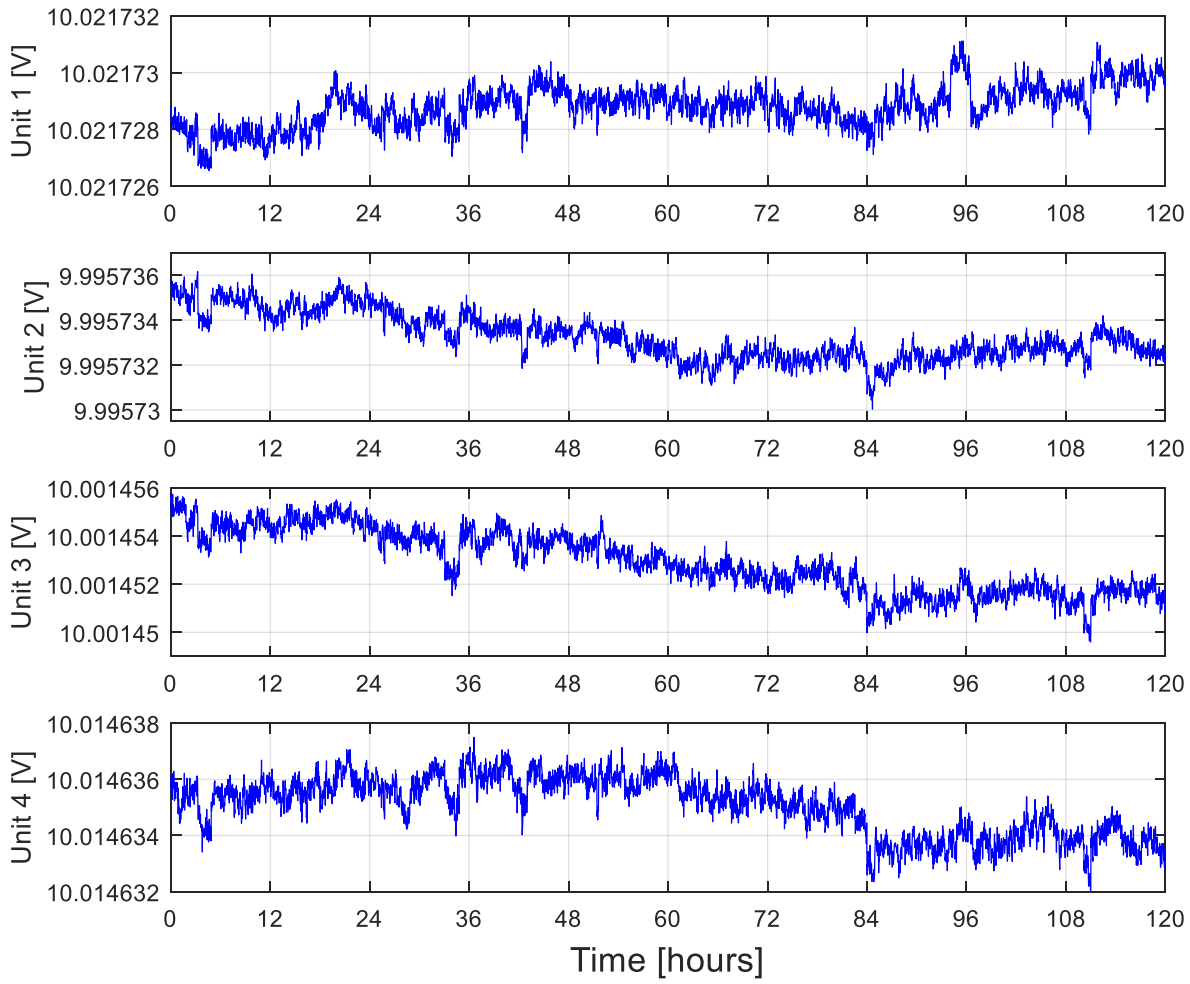

Fig. 3. 12-hour stability measurement against a single PBC

Table 2 gives peak-to-peak results for a sliding and overlapping 12-hour window taken over the 5-day data for the 4 units. Note that the given noise is not fully determined by the ADCs, as the PBC noise contributes as well. There may also be a temperature-related component. Due to setup limitations, all ADCs were operated without internal temperature regulation.

Table 2. 12-hour peak-to-peak values derived from the data shown in Fig. 3

Unit	12-hour stability [ppm p-p]
1	0.27 ± 0.052
2	0.266 ± 0.047
3	0.261 ± 0.05
4	0.287 ± 0.043

Table 3 gives the matrix of normalized correlation coefficients between the measurements. Even a visual inspection of Fig. 3 reveals that Units 2 and 3 are highly coherent. Although the correlation coefficients cannot be used to reliably determine the contribution of the PBC, they do suggest that the measured noise is not simply the independent contribution of each ADC.

Table 3. Normalized correlation coefficients for the measurements shown in Fig. 3

Unit	1	2	3	4
1	1	-0.2411	-0.3235	-0.1057
2	-0.2411	1	0.8330	0.5177
3	-0.3235	0.8330	1	0.7654
4	-0.1057	0.5177	0.7654	1

3. Linearity

Linearity was measured using a Datron 4808 calibrator and four 3458A DVMs. Measurement points were spaced by 0.1 V, leading to a total of 201 points for the -10 to +10 V range. Results are given in Fig. 4 and Table 4.

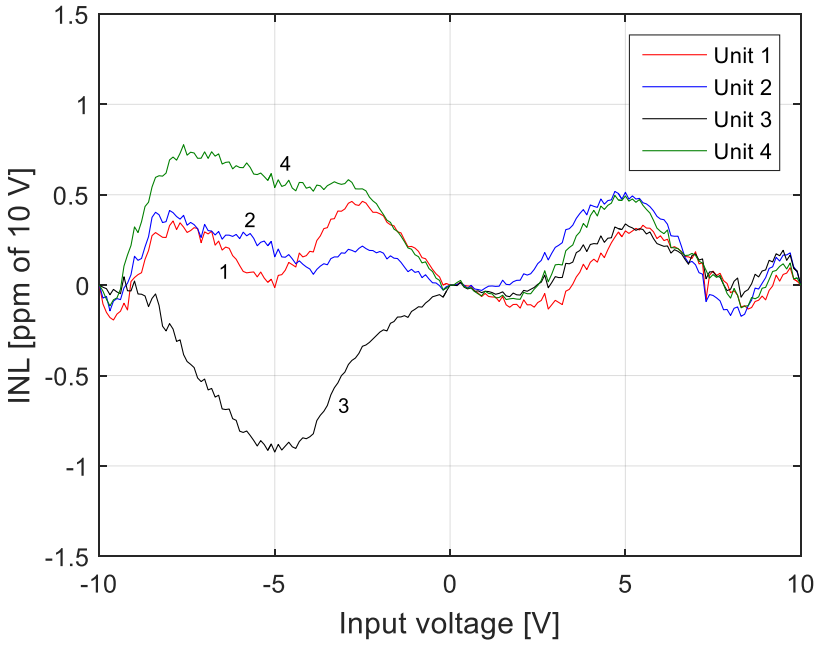

Fig. 4. Integral non-linearity from -10 V to +10 V

Table 4. Worst INL points

Unit	Positive INL (0 to +10 V)		Negative INL (-10 V to 0)	
	INL [ppm]	at input [V]	INL [ppm]	at input [V]
1	0.33 ± 0.08	5.5	0.46 ± 0.06	-2.5
2	0.52 ± 0.07	4.7	0.41 ± 0.09	-8
3	0.34 ± 0.08	5	-0.92 ± 0.08	-5
4	0.49 ± 0.08	5	0.78 ± 0.09	-7.6

The given type B uncertainty is derived from the 3458A 10 V transfer accuracy of 0.05 + 0.05 (ppm of reading + ppm of range). The uncertainty is conservative and does not take into account the fact that 4 DVM readings were averaged. On the other hand, we cannot assume that the linearity of the DVMs is completely independent. Thus, the given uncertainty is for the worst-case scenario of completely similar INL of the 4 DVMs. In the best-case scenario, INL is fully uncorrelated, and the uncertainties would be 2 times lower.

4. Temperature drift

Temperature drift was measured in the oven at two ambient temperature setpoints: 25 °C and 35 °C. The measurement cycles typically took 5-6 hours after overnight settling at 25 °C.

4.1 Without temperature regulation

Results are given in Table 5. All units were measured simultaneously.
Unit 1 had lower temperature drift before the replacement of the resistor array RN2. The observed higher drift is likely due to the manual soldering of the array.

Table 5. Offset and gain drift measured without temperature regulation

Unit	Offset drift [ppm/°C]	Gain drift [ppm/°C]
1	+0.041 ± 0.0024	+1.80 ± 0.014
2	+0.132 ± 0.0025	+0.303 ± 0.0056
3	-0.078 ± 0.0019	+0.684 ± 0.0047
4	-0.045 ± 0.0022	+0.957 ± 0.0079

4.2 With temperature regulation

Results are given in Table 6. Measurements were taken on 2 units at a time due to limitations in the measurement setup.
Note the different unit (**ppb** per degree C) and the much higher measurement uncertainty.

Table 6. Offset and gain drift measured with temperature regulation

Unit	Offset drift [ppb/°C]	Gain drift [ppb/°C]
1	+17 ± 2.7	-32 ± 5.7
2	+6.5 ± 2.2	+30 ± 4.9
3	+4.6 ± 2.1	+9.5 ± 5.5
4	+14 ± 2.2	-5.7 ± 6

4.3 Performance of the temperature regulation system

The behaviour of the temperature regulation system was studied in several different ways.

First, the power consumption of the ADC mezzanine board was measured. It was found to be approximately 1 W. When no heating or cooling was provided by the Peltier element, the temperature on the board increased by about 22 °C, yielding thermal resistance of 22 K/W against the ambient environment.

Fig. 5 shows the needed Peltier current and power to remove the 1 W of heat load at different ambient temperatures, when regulating at $T_{setpoint}$ = 40 °C. In the shown range, the Peltier element operates only in cooling mode. Below about 23 °C it would need to provide heating in order to maintain the same temperature setpoint.

The shown measurements are a good guideline for dimensioning the power supply for the HPM7177. Further tests are needed to assess the performance of the temperature regulation system. However, so far it appears to be robust and efficient.

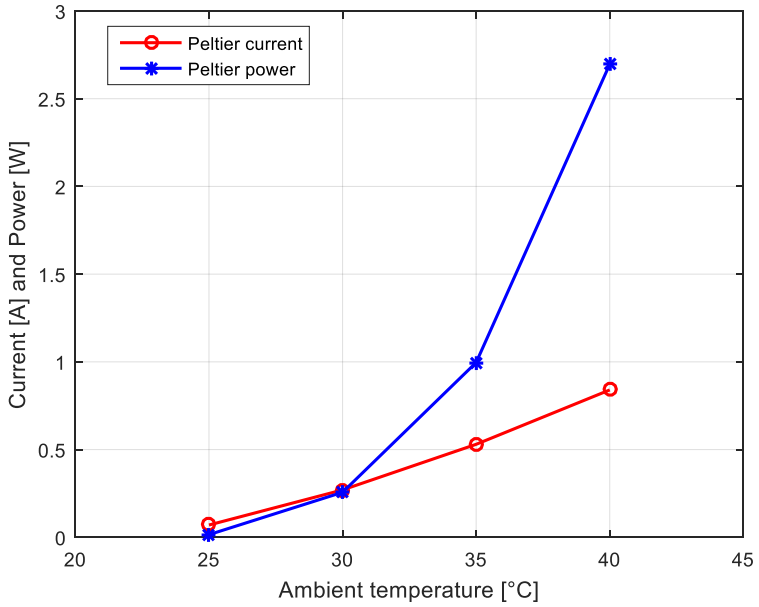

Fig. 5. Peltier current and power versus ambient temperature

5. Common-mode rejection

All units were CMRR-trimmed. The measurements shown on Fig. 6 were taken from Unit #2. The following tuning procedure was used:

1. Observe the output of branch A and tune P2 for maximum CMRR
2. Observe the differential output (branch A – branch B) and tune P1 to maximize the total CMRR

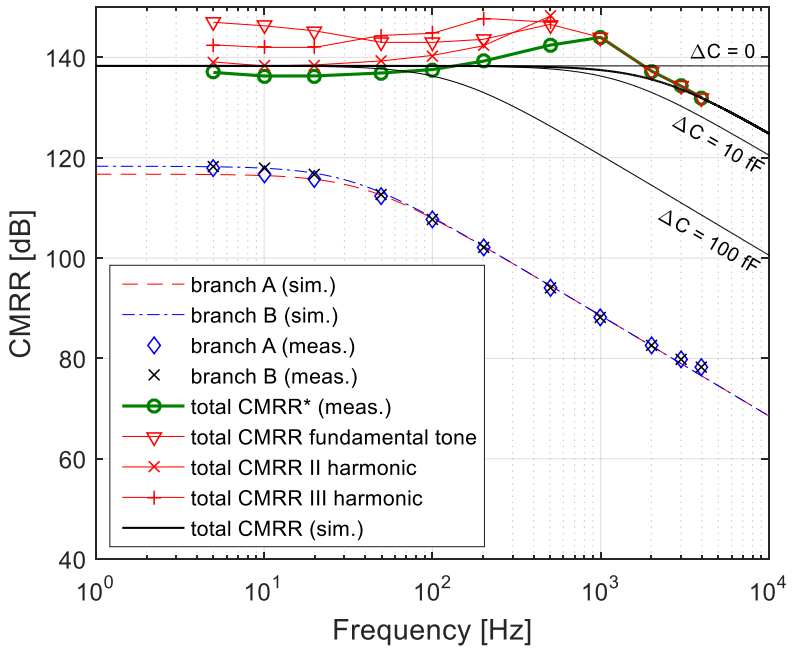

Fig. 6. Measured and simulated CMRR

Further details on the CMRR simulations and explanation for the excellent behaviour of the circuit will be provided in a separate document.

6. Power supply rejection

Power supply rejection at DC was studied by varying the +15 V, -15 V and +5 V supply lines. No measurable effect was observed when measurements were taken at 0 V (external short). A small effect was seen when measuring +10 V from a PBC. The ADC reading showed sensitivity to variations in the +15 V supply on the order of 0.1 ppm/V. It is most likely related to the LTZ1000 reference circuit, which is powered directly from the +15 V rail. The only other analog circuits that use this rail (and -15 V as well) are the input multiplexer and buffers based on OPA189.

7. Settling to multiplexer-selected voltages

The internal multiplexer was used to study how the ADC settles to voltage steps (Fig. 7). The worst settling is seen when switching from 0 to +10 V or to -10 V. It is approximately 0.1 ppm with time constant in the tens of seconds. The effect is purely thermal, as confirmed by the measurable reaction of the temperature regulation loop to the voltage steps.

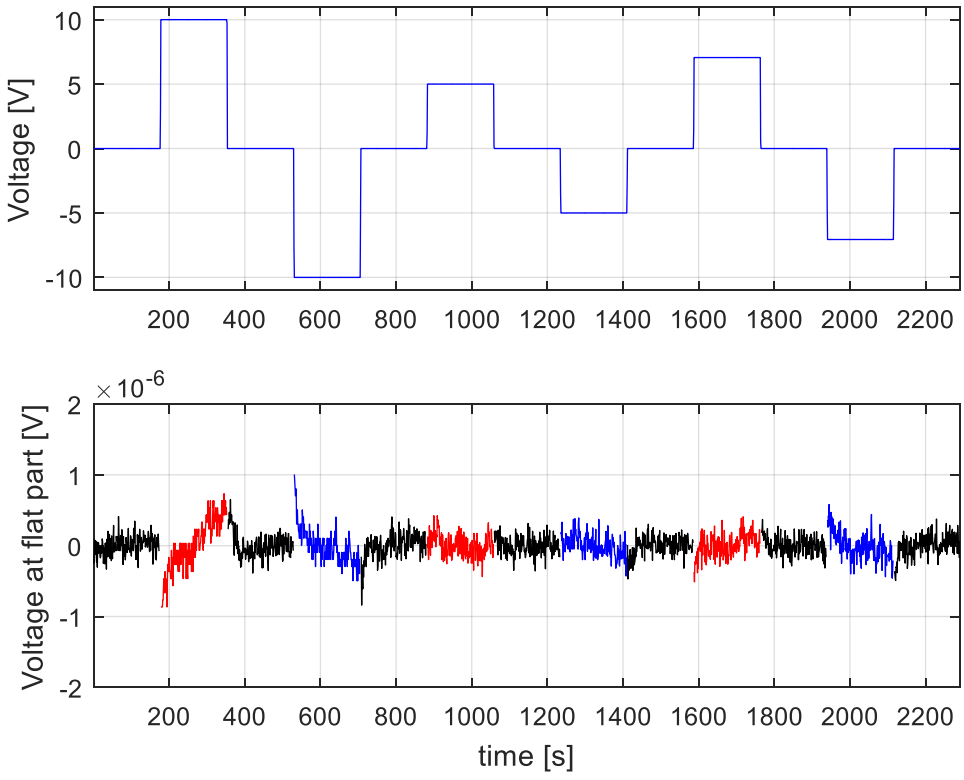

Fig. 7. Settling to voltages selected by the MUX

8. Identified problems and issues to improve

8.1 Oscillation in Vref buffer

The Vref buffer sub-circuit (Fig. 8) was found to be unstable under certain conditions. It exhibited sustained oscillation with $f \approx 1$ MHz. The oscillation was not present at start-up, but was triggered

by a step in the measured ADC voltage. This mechanism suggests it was related to the dynamic loading on the Vref pin of the ADC (not shown on Fig 8).

Replacing IC6 with ADA4522-1 solves the problem without compromising the DC performance. ADA4522-1 has about 5 times lower GBP than OPA189 and very similar temperature drift and noise.

Another possible solution for the future is to use OPA189 with additional compensation within the composite amplifier. The use of OPA189 is desirable in order to keep the BOM smaller.

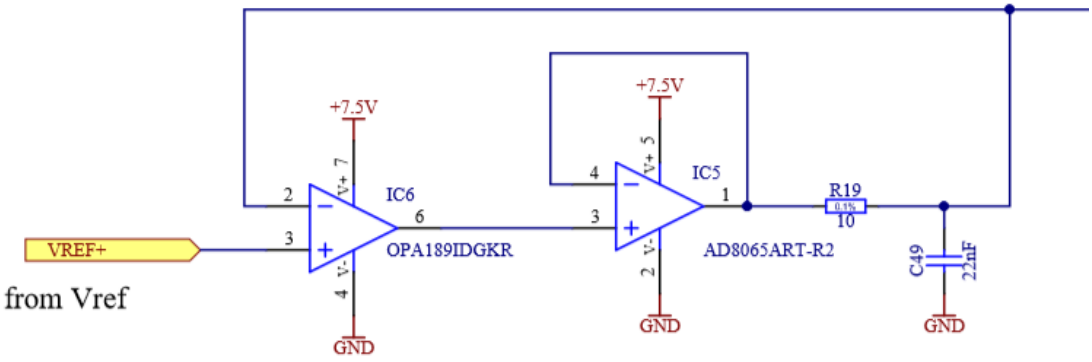

Fig. 8. Vref buffer sub-circuit

8.2 Oscillation in 10 V ref voltage

A more subtle oscillation problem was found in the 10 V reference sub-circuit (Fig. 9).

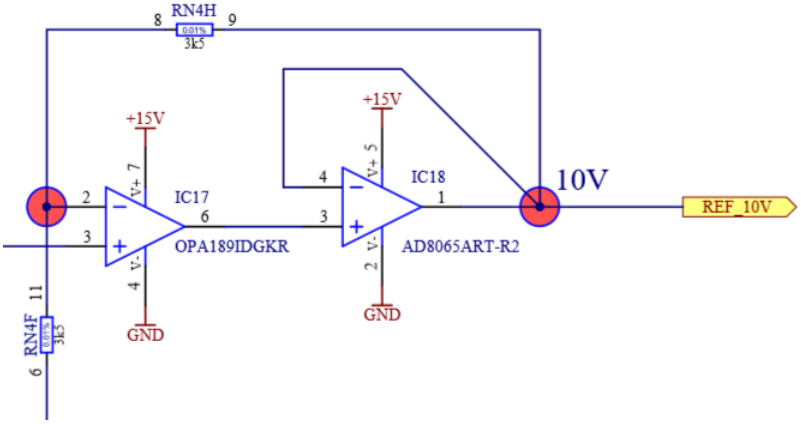

Fig. 9. 10 V reference sub-circuit

The oscillation was present at start-up. Its frequency depended on the coupling of REF_10V to the input multiplexer (there is no other loading of this voltage line). The oscillation frequency was very high. Depending on the loading, it varied from 62 to 71 MHz.
It was eventually determined that the instability was caused by parasitic loading of IC18. The load was a thin PCB trace leading from IC18 to the multiplexer. It formed a parasitic tuned LC circuit that determined the oscillation frequency. Introducing a 100 Ω resistor at the output of IC18 solved the problem.

8.3 ADC Supply voltage AVDD1

LTZ1000 has considerable spread of the Zener voltage. With the present voltage reference scaling circuit, the 5 V provided for the AD7177-2 is actually slightly higher than 5 V. In order

to meet the datasheet requirement that V_{REF} < AVDD1 + 50 mV, the 5V supply was increased in all units by adding parallel resistor to R2 on the mainboard (EDA-04060-V1).

8.4 Problems in Unit #1

Initital tests showed a big offset voltage in Unit 1 on the order of 20 mV. It was traced to one element in the resistor array RN2, which had a value far from the nominal and severely out of specs (3430 Ω instead of 3500 Ω).

RN2 was replaced to fix the problem. However, the repaired unit showed considerably higher temperature drift in later measurements. The increase is probably related to the manual soldering of the part.

In addition, another problem was found in the unit while tuning its CMRR. At negative CM voltages of -5 V or more, the signal became distorted and noisy. This effect is probably due to a damaged operational amplifier. It could be related to the resistor array problem, or the two problems could point to a single issue related to the fabrication of this particular unit.

8.5 Galvanic connection between GND and the chassis

It was found that GND was connected to the chassis on all units through the mounting screws of the backplane connector J3 on the mainboard. The problem was solved by removing all screws and isolating the board with tape. In the future, the PCB should be modified to remove the unwanted connection.

8.6 Offset drift of the ADC with internal short

The drift of the ADC alone with internal MUX short was measured in order to separate the contribution of the attenuator circuit. It was also done as a sanity check.
It was found that the drift was too high to be explained by the AD7177-2 offset drift as stated in the datasheet. Moreover, it was consistent between the 4 units, having the same sign and similar magnitude (Table 7).

Many tests were carried out to find the origin of this drift, but nothing conclusive was found. It should be noted that the drift is still very low. It is practically unmeasurable when temperature regulation is enabled.

Table 7. ADC offset drift measured without temperature regulation

Unit	ADC offset drift [ppb/°C]
1	+54.6 ± 2.3
2	+45.4 ± 1.8
3	+62.8 ± 1.5
4	+57.8 ± 1.8

9. Conclusions

No major flaws were found in the design of HPM7177. The performance of 4 units meets all HL-LHC Class 0 performance requirements, with the exception of Unit #3 that has INL too close to the limit. However, if we consider only the positive-side INL, and since the Class 0 circuits are unipolar, then this unit also qualifies easily. Furthermore, positive INL appears to be much more consistent between the 4 units. The discrepancy in negative INL should be investigated further,

as it is possible that a hardware remedy exists. LUT-based linearization remains to be demonstrated in practice as well, regardless of whether it will be implemented in the field.

The hardware tests revealed some minor problems and issues to be solved in future versions. They are all listed within this document.

Careful studies of temperature drift in a number of internal voltages revealed that there is no dominant source. When temperature regulation is applied, the improvement is not consistent between the units, and sometimes even leads to sign reversal (see Table 5 and Table 6). This fact points to one of two possible explanations:

1) The temperature regulation system performs extremely well and suppresses all drifts to unmeasurably low values. Then the remaining TC is determined by the imperfection of the temperature measurement itself;
2) The regulation system acts differently on the various contributors (ADC, attenuator, Vref scaling circuit, etc). Thus, it interacts in non-trivial ways with the statistical spread of their TCs and ultimately their weighed sum.

In either case, the findings are very positive. They prove that there are no major mistakes in the circuits and the thermal design of the system. The measured performance of the 4 units provides high degree of confidence for meeting the TC requirements in series production.

This report will be completed with more measurement data in 2020. In addition to further INL tests and evaluation of the temperature controller, the devices will be tested in the CERN EMC lab for EMI susceptibility. Characterization measurements against the 10 V Programmable Josephson Array Standard at PTB-Braunschweig are also planned.

10. Appendix

The following measurement files were used to produce the data presented in this document:

- Temperature drift without regulation
  281119a.txt (unit order 4-3-2-1; 25 °C: 1-700 s; 35 °C: 1600-2000 s)

- Temperature drift with regulation
  Units 1 and 2: 021219a.txt (unit order 1-2-3-4; 25 °C: 1-700 s; 35 °C: 1600-2200 s)
  Units 3 and 4: 031219a.txt (unit order 4-3-2-1; 25 °C: 1-700 s; 35 °C: 1600-2200 s)

- INL
  181119i.txt (unit order 4-3-2-1)

- Noise spectra - Unit #2

  Shorted inputs
  0.001 to 50 Hz: 181119a.txt
  0.1 to 5000 Hz: 181119c.txt

  Internal ADC short
  0.001 to 50 Hz: 251119a.txt
  0.1 to 5000 Hz: 251119c.txt

  LF noise with PBC
  0.001 to 50 Hz: 161219c.txt

- 12-hour stability of all 4 units measured over 5 days:
  161219a.txt (unit order: 4-3-2-1)